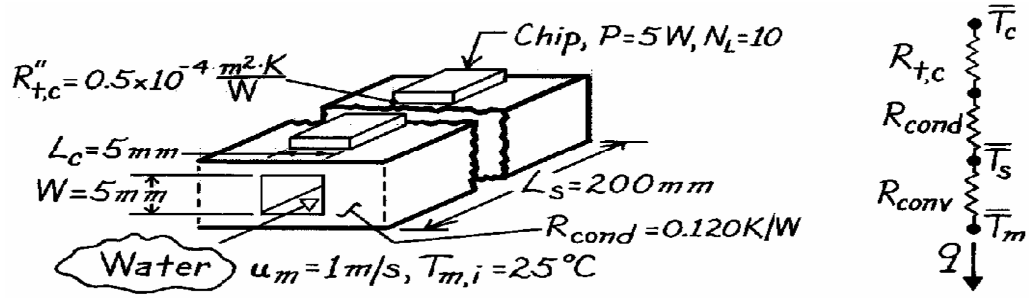
PROBLEM 8.113

KNOWN: Arrangement of chips and cooling channels for a substrate. Contact and conduction resistances. Coolant velocity and inlet temperature.

FIND: (a) Coolant temperature rise, (b) Chip and substrate temperatures.

SCHEMATIC:



ASSUMPTIONS: (1) Constant properties, (2) Fully-developed flow, (3) Incompressible liquid with negligible viscous dissipation, (4) Heat transfer exclusively to water, (5) Steady-state conditions.

PROPERTIES: Water (given): $\rho = 1000\ \text{kg/m}^3$, $c_p = 4180$ J/kg·K, k = 0.610 W/m·K, Pr = 5.8, $\mu = 855 \times 10^{-6}$ kg/s·m.

ANALYSIS: (a) For a single flow channel, the overall energy balance yields

$$T_{m,o} - T_{m,i} = \frac{q}{\dot{m}\, c_p} = \frac{N_L P}{\rho\, u_m A_c c_p} = \frac{10 \times 5\ \text{W}}{1000\ \text{kg/m}^3 \left(1\ \text{m/s}\right)\left(0.005\ \text{m}\right)^2 4180\ \text{J/kg}\cdot\text{K}} = 0.48^\circ\text{C}. \quad <$$

From the thermal circuit,

$$q = \frac{T_o - \overline{T}_m}{R_{t,c} + R_{cond} + R_{conv}} \qquad R_{t,c} = R''_{t,c} / A_s = \left(0.5 \times 10^{-4}\ \text{m}^2 \cdot \text{K/W}\right) / 10\left(0.005\ \text{m}\right)^2 = 0.2\ \text{K/W}.$$

With $D_h = 4A_c/P = 4(0.005\ \text{m})^2/4(0.005\ \text{m}) = 0.005$ m,

$$Re_D = \frac{\rho\, u_m D_h}{\mu} = \frac{1000\ \text{kg/m}^3 \left(1\ \text{m/s}\right) 0.005\ \text{m}}{855 \times 10^{-6}\ \text{kg/s}\cdot\text{m}} = 5848.$$

With turbulent flow, the Gnielinski correlation yields

$$h = \frac{k}{D}\frac{(f/8)(Re_D - 1000)\,Pr}{1 + 12.7(f/8)^{1/2}(Pr^{2/3} - 1)} = \frac{0.61\text{W/m}\cdot\text{K}}{0.005\text{m}}\frac{(0.0368/8)(5848 - 1000)5.8}{1 + 12.7(0.0368/8)^{1/2}(5.8^{2/3} - 1)} = 5406\text{W/m}^2\cdot\text{K}$$

where $f = (0.79 \ln Re_D - 1.64)^{-2} = 0.0368$.

$$R_{conv} = \left(hA_s\right)^{-1} = \left(5406\ \text{W/m}^2 \cdot \text{K} \times 4 \times 0.005\ \text{m} \times 0.2\ \text{m}\right)^{-1} = 0.046\ \text{K/W}.$$

Approximating T_m as $(T_{m,i} + T_{m,o})/2 = 25.24$°C,

$$\overline{T}_c = \overline{T}_m + q\left(R_{t,c} + R_{cond} + R_{conv}\right) = 25.24^\circ\text{C} + 50\ \text{W}\left(0.2 + 0.12 + 0.046\right)\text{K/W} = 43.6^\circ\text{C}. \quad <$$

Similarly, from the thermal circuits,

$$\overline{T}_s = \overline{T}_m + q \times R_{conv} = 25.24^\circ\text{C} + 50\text{W} \times 0.046\text{K/W} = 27.6^\circ\text{C} \quad <$$

COMMENTS: (1) Since the coolant temperature rise is less than 0.5°C, all chip temperatures will be within 0.5°C of each other. (2) The channel surface temperature may also be obtained from Eq. 8.41b, yielding the same result.